

IN THE CLAIMS:

1-30. Canceled

31. (Currently Amended) An apparatus, comprising:
a first input clock digital phase-locked loop;
a second input clock digital phase-locked loop;
a stratum clock state machine coupled to the first input clock digital phase-locked loop
and to the second input clock digital phase-locked loop; and
a main clock phase-locked loop coupled to the first input clock digital phase-locked loop,
to the second input clock digital phase-locked loop and to the stratum clock state
machine.
32. (Original) The apparatus of claim 31, wherein the stratum clock state machine can define a
holdover state in which a phase buildout function is active.
33. (Original) The apparatus of claim 32, wherein the stratum clock state machine can define a
normal state, an offset state, a switch state and a freerun state.
34. (Original) The apparatus of claim 31, further comprising a numerically controlled oscillator
coupled to the main clock phase-locked loop.
35. (Original) The apparatus of claim 34, further comprising a phase and frequency detector
coupled to the numerically controlled oscillator.
36. (Original) The apparatus of claim 35, further comprising an oven controlled crystal
oscillator, coupled to the phase and frequency detector.

37. (Original) The apparatus of claim 36, further comprising a temperature sensor coupled to the oven controlled crystal oscillator and to the stratum clock state machine.
38. (Original) The apparatus of claim 35, further comprising a loop filter coupled to the phase and frequency detector.
39. (Original) The apparatus of claim 38, wherein the loop filter includes a programmable filter.
40. (Original) The apparatus of claim 39, wherein the programmable filter is coupled to the stratum clock state machine.
41. (Original) The apparatus of claim 38 further comprising a voltage controlled oscillator coupled to the loop filter, to the first input clock digital phase-locked loop and to the second input clock digital phase-locked loop.
42. (Original) The apparatus of claim 41, further comprising:
an output buffer coupled to the voltage controlled oscillator; and
a clock divider coupled to the voltage controlled oscillator and to the output buffer.
43. (Original) The apparatus of claim 31, further comprising an eight bit parallel bus coupled to the stratum clock state machine.
44. (Original) The apparatus of claim 31, further comprising a simple logic interface coupled to the stratum clock state machine.
45. (Original) A method comprising deploying the apparatus of claim 31.
46. (Original) A kit, comprising the apparatus of claim 31.
47. (Original) The kit of claim 46, further comprising instructions.

48. (Original) A method comprising deploying the kit of claim 46.